US012047480B2

(12) **United States Patent**
Mahany et al.

(10) **Patent No.: US 12,047,480 B2**
(45) **Date of Patent: Jul. 23, 2024**

(54) **EtherCAT DEVICE**

(71) Applicant: **Microchip Technology Incorporated**, Chandler, AZ (US)

(72) Inventors: **William Mahany**, West Islip, NY (US); **Ian Saturley**, Warwickshire (GB); **Lakshmi Narasimhan**, Chennai (IN); **Riyas Kattukandan**, Kerala (IN); **Ramya Kuppusamy**, Karnataka (IN); **Robert Zakowicz**, Chandler, AZ (US)

(73) Assignee: **Microchip Technology Incorporated**, Chandler, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **18/125,857**

(22) Filed: **Mar. 24, 2023**

(65) **Prior Publication Data**

US 2023/0231938 A1 Jul. 20, 2023

Related U.S. Application Data

(62) Division of application No. 17/030,439, filed on Sep. 24, 2020, now Pat. No. 11,924,312.

(30) **Foreign Application Priority Data**

Oct. 30, 2019 (IN) 201911043952

(51) **Int. Cl.**
H04L 69/22 (2022.01)
G06F 9/4401 (2018.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H04L 69/22*** (2013.01); ***G06F 9/4418*** (2013.01); ***H04J 3/0658*** (2013.01); ***H04L 12/10*** (2013.01)

(58) **Field of Classification Search**
CPC H04L 69/22; H04L 12/10; G06F 9/4418; H04J 3/0658
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,914,957 A 6/1999 Dean et al. 370/438
7,843,218 B1 11/2010 Ramaraju et al. 326/46
(Continued)

FOREIGN PATENT DOCUMENTS

CN 1212540 A 3/1999 ..... B66B 3/00
CN 104348690 A 2/2015 ..... H04L 12/10
(Continued)

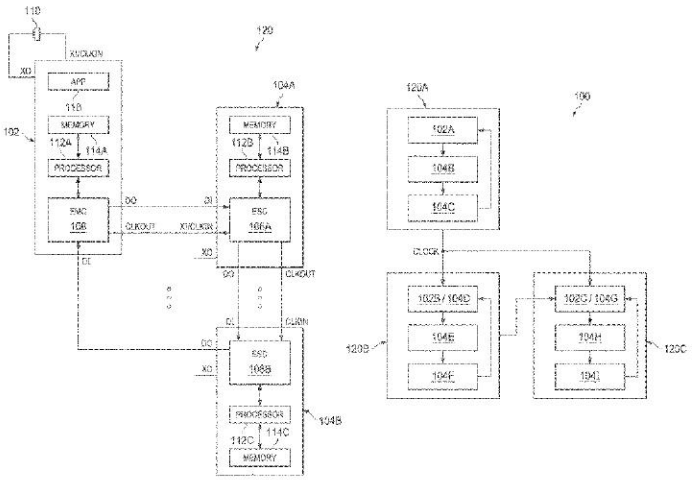
OTHER PUBLICATIONS

Partial International Search Report and Invitation to Pay Additional Fees, Application No. PCT/US2020/057292, 13 pages, Feb. 11, 2021.

(Continued)

Primary Examiner — Samina F Choudhry
(74) *Attorney, Agent, or Firm* — SLAYDEN GRUBERT BEARD PLLC

(57) **ABSTRACT**

An EtherCAT device is disclosed. The EtherCAT device comprises a data input port to receive a signal representing data, the signal representing one of a plurality of possible logical values; and a degradation calculation circuit. The degradation calculation circuit is to read, demodulate, and convert the received signal into a digital domain representation; process the digital domain representation into slices, where the value of the received signal at a respective time is represented in a respective one of the slices; determine differences between the respective slices and reference slices; identify an intended logical value of the received signal responsive to the determined differences; determine a quantification of error at the respective time responsive to the identified logical value and the determined differences;

(Continued)