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[54] **PREMATURE TERMINATION OF MICROCONTROLLER EEPROM WRITE**

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[58] **Field of Search** 365/230.01, 228; 235/380, 487; 364/483, 228; 395/425; 371/15.1, 29.1

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[57] **ABSTRACT**

A single chip, semiconductor microcontroller device is adapted to control an aspect of the operation of an external system. The device includes a CPU, program memory for storing instructions to be selectively executed by the CPU to perform the control functions, and peripheral EEPROM data memory adapted to be written to for storing selected data in selected ones of a multiplicity of addresses of the data memory and for selective retrieval of the stored dam by the CPU within its control function. Internal logic in the device is implemented to abort a write operation in progress on the EEPROM data memory upon occurrence of an asynchronous reset of the device. An error flag is set by the logic to indicate that the write operation is being aborted, and the data that was partially written to the EEPROM memory at the time the write operation was aborted is held intact.

7 Claims, 1 Drawing Sheet

