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[54] **METHOD AND APPARATUS FOR TESTING A RELATIVELY SLOW SPEED COMPONENT OF AN INTERGRATED CIRCUIT HAVING MIXED SLOW SPEED AND HIGH SPEED COMPONENTS**

[75] Inventors: **Randy Yach**, Phoenix, Ariz.; **Rodney Drake**, Phoenix, Ariz.

[73] Assignee: **Microchip Technology Incorporated**, Chandler, Ariz.

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[52] **U.S. Cl.** **371/22.1**

[58] **Field of Search** 371/22.1, 21.1, 371/22.2; 365/201; 345/87

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Primary Examiner—Hoa T. Nguyen

Attorney, Agent, or Firm—Blank Rome Comisky & McCauley LLP

[57] **ABSTRACT**

A method is disclosed for testing a high speed microcontroller fabricated on a semiconductor chip, and for testing relatively low speed functions of a liquid crystal display (LCD) module on the chip that drives an off-chip LCD for an external system to be controlled by the microcontroller with a plurality of discrete analog voltage levels for performing the LCD functions. Digital values are multiplexed in time slots of a test waveform to simulate in high speed digital format of a test mode the low speed timing, relative magnitude and functionality of analog voltage levels used to drive the LCD; A high speed driver is selectively coupled to a pin of the chip, to which the discrete analog voltage levels are normally applied at low speed to drive the LCD, and the test waveform is applied to the high speed driver. The digital values and timing that appear on the pin are then monitored as an indication of proper functionality of the LCD module. The high speed driver is switched out and the normal low speed LCD driver is switched back for return to an LCD user mode when the test mode is completed. Monitoring the pin with a digital tester allows verification that pin pulses in predetermined time slots indicate the corresponding analog voltage level is being applied at the proper time during normal operation of the LCD module, and digitally testing of continuity in an analog channel. A transistor normally employed on the chip for electrostatic discharge protection is activated to selectively couple the high speed driver to the pin for the high speed testing mode.

6 Claims, 10 Drawing Sheets

