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St. Amand et al.

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[54] **METHOD OF FORMING NARROW THERMAL SILICON DIOXIDE SIDE ISOLATION REGIONS IN A SEMICONDUCTOR SUBSTRATE AND MOS SEMICONDUCTOR DEVICES FABRICATED BY THIS METHOD**

[75] Inventors: **Roger D. St. Amand**; **Neil F. Deutscher**, both of Temple; **Robert P. Ma**, Phoenix, all of Ariz.

[73] Assignee: **Microchip Technology Incorporated**, Chandler, Ariz.

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[52] **U.S. Cl.** **438/294**; 438/297

[58] **Field of Search** 438/410, 439, 438/448, 294, 297, 295

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,534,824 8/1985 Chen 156/628

4,871,685 10/1989 Taka et al. 437/33

5,580,815 12/1996 Hsu et al. .

Primary Examiner—Joni Chang

Attorney, Agent, or Firm—Harry M. Weiss; Harry M. Weiss & Associates, P.C.

[57] **ABSTRACT**

A method is disclosed for forming narrow thermal silicon dioxide side isolation regions in a semiconductor substrate and MOS or CMOS semiconductor devices fabricated by this method. A thin oxynitride lateral diffusion barrier to oxygen is used in conjunction with a polysilicon buffering stress relief layer on the surface of a semiconductor substrate prior to the field oxidation process to restrict lateral silicon dioxide expansion thereby permitting the creation of narrow thermal silicon dioxide side isolation regions in the semiconductor substrate.

10 Claims, 4 Drawing Sheets

