US006055211A

United States Patent [19]

Yach

[11] Patent Number: 6,055,211

[45] Date of Patent: Apr. 25, 2000

[54] **FORCE PAGE ZERO PAGING SCHEME FOR MICROCONTROLLERS USING DATA RANDOM ACCESS MEMORY**

[75] Inventor: **Randy L. Yach**, Phoenix, Ariz.

[73] Assignee: **Microchip Technology Incorporated**, Chandler, Ariz.

[21] Appl. No.: **08/887,876**

[22] Filed: **Jul. 3, 1997**

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/238.5**; 365/239

[58] **Field of Search** 365/238.5, 235, 365/239, 240; 395/800.01, 800.32, 800.33

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,255,382	10/1993	Pawloski	395/425
5,809,327	9/1998	Wollan et al.	395/800.33
5,887,189	3/1999	Birns et al.	395/800.32

Primary Examiner—David Nelms
Assistant Examiner—David Lam
Attorney, Agent, or Firm—Ronald L. Chichester; Paul N. Katz; Frohwitter

[57] **ABSTRACT**

A microcontroller architecture that adds a dedicated bit in the op-code decode field to force data access to take place on page 0 of the random access memory (RAM) for that instruction. This allows the user to have any page selected and still have direct access to the special function registers or the register variables which are located on page 0 of the RAM. The setting of the dedicated bit will not affect the current operation of the microcontroller nor will the setting of the bit modify the currently selected address stored in the op-code instruction currently being executed by the microcontroller.

13 Claims, 2 Drawing Sheets

