US006728856B2

(12) **United States Patent**
Grosbach et al.

(10) **Patent No.: US 6,728,856 B2**
(45) **Date of Patent: Apr. 27, 2004**

(54) **MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING PROGRAM MEMORY SPACE MAPPED TO DATA MEMORY SPACE**

(75) Inventors: **James H. Grosbach**, Scottsdale, AZ (US); **Joshua M. Conner**, Apache Junction, AZ (US); **Michael Catherwood**, Pepperell, MA (US)

(73) Assignee: **Microchip Technology Incorporated**, Chandler, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 305 days.

(21) Appl. No.: **09/870,648**

(22) Filed: **Jun. 1, 2001**

(65) **Prior Publication Data**

US 2002/0184465 A1 Dec. 5, 2002

(51) **Int. Cl.**[7] **G06F 12/02**
(52) **U.S. Cl.** **711/202**
(58) **Field of Search** 712/35, 37–40; 711/202

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,781,810	A	12/1973	Downing	712/228
4,398,244	A	8/1983	Chu et al.	712/244
4,472,788	A	9/1984	Yamazaki	708/209
4,481,576	A	11/1984	Bicknell	711/217
4,488,252	A	12/1984	Vassar	708/505
4,511,990	A	4/1985	Hagiwara et al.	708/501
4,556,938	A	12/1985	Parker et al.	712/241
4,626,988	A	12/1986	George	712/241
4,730,248	A	3/1988	Watanabe et al.	712/228
4,782,457	A	11/1988	Cline	708/205
4,807,172	A	2/1989	Nukiyama	708/209
4,829,420	A	5/1989	Stahle	711/200
4,829,460	A	5/1989	Ito	708/209
4,839,846	A	6/1989	Hirose et al.	708/497
4,872,128	A	10/1989	Shimizu	708/209
4,882,701	A	11/1989	Ishii	712/241
4,941,120	A	7/1990	Brown et al.	708/497
4,943,940	A	7/1990	New	708/507
4,959,776	A	9/1990	Deerfield et al.	711/217
4,977,533	A	12/1990	Miyabayashi et al.	708/404
4,984,213	A	1/1991	Abdoo et al.	365/230.03
5,007,020	A	4/1991	Inskeep	711/200
5,012,441	A	4/1991	Retter	711/217
5,032,986	A	7/1991	Pathak et al.	711/217
5,038,310	A	8/1991	Akagiri et al.	708/205
5,056,004	A	10/1991	Ohde et al.	712/241
5,099,445	A	3/1992	Studor et al.	708/209
5,101,484	A	3/1992	Kohn	712/241
5,117,498	A	5/1992	Miller et al.	712/241
5,122,981	A	6/1992	Taniguchi	708/497

Primary Examiner—David L. Robertson
(74) *Attorney, Agent, or Firm*—Swidler Berlin Shereff Friedman, LLP

(57) **ABSTRACT**

A processor has an architecture that provides the processing speed advantages of the Harvard architecture, but does not require special purpose instructions or two separate external memories in order to expand both data memory and program instruction memory. The processor has separate program memory space and data memory space, but provides the capability to map at least a portion of the program memory space to the data memory space. This allows most program instructions that are processed to obtain the speed advantages of simultaneous program instruction and data access, yet provides a means to access program memory resident data without special purpose instructions. It also allows program memory space and data memory space to be expanded externally to the processor using only one external memory device that includes both program instructions and data. The processor includes a program memory space operable to store program instructions and data, a data memory space operable to store data, and mapping circuitry operable to map at least a portion of the program memory space to the data memory space. The program memory space may be internal to the processor. The processor may further comprise a page register operable to specify a location of the program memory space that is mapped to the data memory space.

13 Claims, 4 Drawing Sheets

